

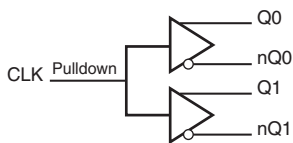
### GENERAL DESCRIPTION

The 85222-02 is a 1-to-2 LVCMOS / LVTTL-to-Differential HSTL translator. The 85222-02 has one single ended clock input. The single-ended clock input accepts LVCMOS or LVTTL input levels and translates them to HSTL levels. The small outline 8-pin SOIC package makes this device ideal for applications where space, high performance and low power are important.

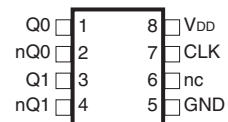
### FEATURES

- Two differential HSTL outputs
- One LVCMOS/LVTTL clock input
- CLK input can accept the following input levels: LVCMOS or LVTTL
- Maximum output frequency: 350MHz
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 1.25ns (maximum)
- $V_{OH}$ : 1.4V (maximum)
- Output crossover voltage: 0.68V - 0.9V
- Full 3.3V operating supply voltage
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in lead-free RoHS compliant package

### BLOCK DIAGRAM



### PIN ASSIGNMENT



**85222-02**

**8-Lead SOIC**

3.90mm x 4.92mm x 1.37mm body package

**M Package**

Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. HSTL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. HSTL interface levels.
5	GND	Power		Power supply ground.
6	nc	Unused		No connect.
7	CLK	Input	Pulldown	LVC MOS / LV TTL clock input.
8	V <sub>DD</sub>	Power		Positive supply pin.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

NOTE: Unused output pairs must be terminated.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	112.7°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				50	mA

**TABLE 3B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	CLK $V_{DD} = V_{IN} = 3.465V$			150	$\mu A$
$I_{IL}$	Input Low Current	CLK $V_{DD} = 3.465, V_{IN} = 0V$	-5			$\mu A$

**TABLE 3C. HSTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		1.0		1.4	V
$V_{OL}$	Output Low Voltage; NOTE 1		0		0.4	V
$V_{OX}$	Output Crossover Voltage		0.68		0.9	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6	1.0	1.4	V

NOTE 1: All outputs must be terminated with 50 $\Omega$  to ground.

**TABLE 4. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				350	MHz
$t_{PD}$	Propagation Delay; NOTE 1		0.85	1.05	1.25	ns
tsk(o)	Output Skew; NOTE 2, 3				25	ps
tsk(pp)	Part-to-Part Skew; NOTE 4				250	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	250		500	ps
odc	Output Duty Cycle	$f \leq 250MHz$	45		55	%
		$f > 250MHz$	40		60	%

All outputs must be terminated with 50 $\Omega$  to ground.

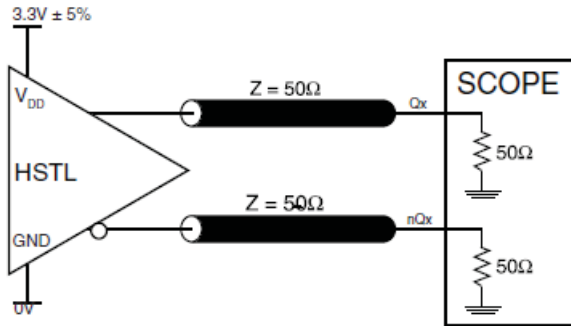
NOTE 1: Measured from  $V_{DD}/2$  of the input to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

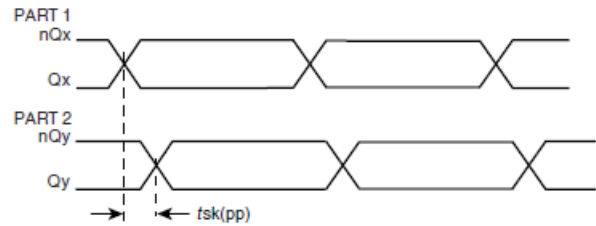
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

# PARAMETER MEASUREMENT INFORMATION

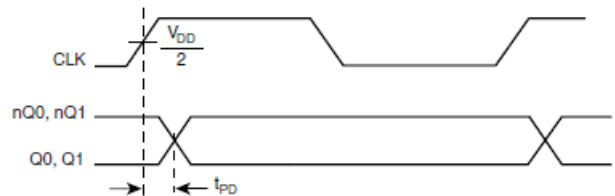
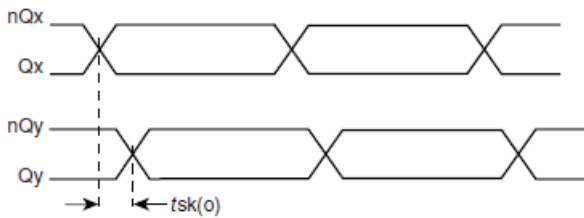


NOTE: All outputs must be terminated with 50Ω to ground.



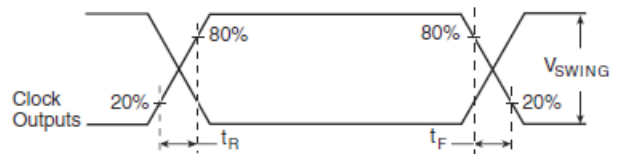
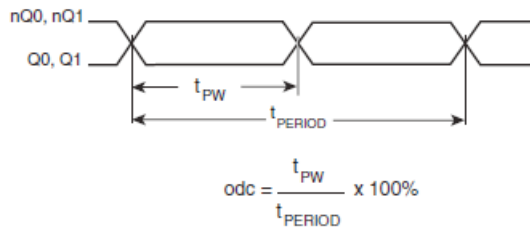
## 3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT

## PART-TO-PART SKEW



## OUTPUT SKEW

## PROPAGATION DELAY



## OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

## OUTPUT RISE/FALL TIME

# APPLICATION INFORMATION

## RECOMMENDATIONS FOR UNUSED OUTPUT PINS

### OUTPUTS:

#### HSTL OUTPUT

All outputs must be terminated with 50Ω to ground.

## SCHEMATIC EXAMPLE

Figure 2 shows a schematic example of 85222-02. In the example, the input is driven by a 7 ohm LVCMOS driver with a series termination. The decoupling capacitor should be physically located

near the power pin. For 85222-02, the unused output need to be terminated.

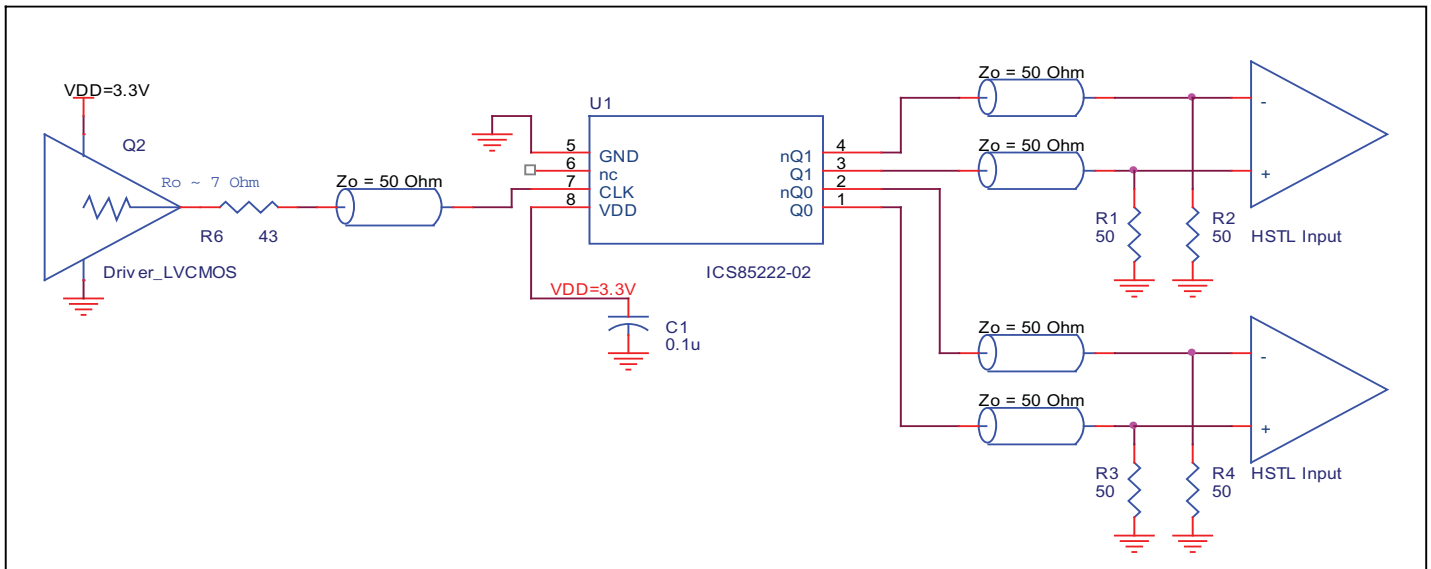


FIGURE 2. 85222-02 HSTL BUFFER SCHEMATIC EXAMPLE

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 85222-02. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 85222-02 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{DD\_MAX} = 3.465V * 50mA = 173.25mW$
- Power (outputs)<sub>MAX</sub> = **73.8mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $2 * 82.3mW = 164.6mW$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 173.25mW + 164.6mW = \mathbf{337.86mW}$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total device power dissipation (example calculation is in Section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per Table 5 below. Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.337W * 103.3^\circ\text{C}/\text{W} = 104.8^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 5. THERMAL RESISTANCE  $\theta_{JA}$  FOR 8-PIN SOIC, FORCED CONVECTION**

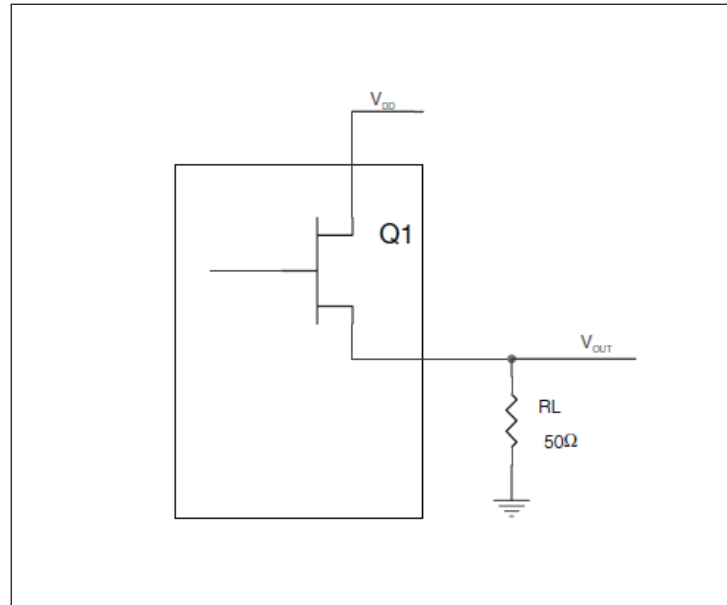
	$\theta_{JA}$ by Velocity (Linear Feet per Minute)		
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 1*.



**FIGURE 1. HSTL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd\_H is power dissipation when the output drives high.

Pd\_L is the power dissipation when the output drives low.

$$Pd\_H = (V_{OH\_MAX} / R_L) * (V_{DD\_MAX} - V_{OH\_MAX})$$

$$Pd\_L = (V_{OL\_MAX} / R_L) * (V_{DD\_MAX} - V_{OL\_MAX})$$

$$Pd\_H = (1.4V / 50\Omega) * (3.465V - 1.4V) = \mathbf{57.8mW}$$

$$Pd\_L = (0.4V / 50\Omega) * (3.465V - 0.4V) = \mathbf{24.52mW}$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = \mathbf{82.3mW}$$

## RELIABILITY INFORMATION

TABLE 6.  $\theta_{JA}$  vs. AIR FLOW TABLE 8 LEAD SOIC

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for 85222-02 is: 411



PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

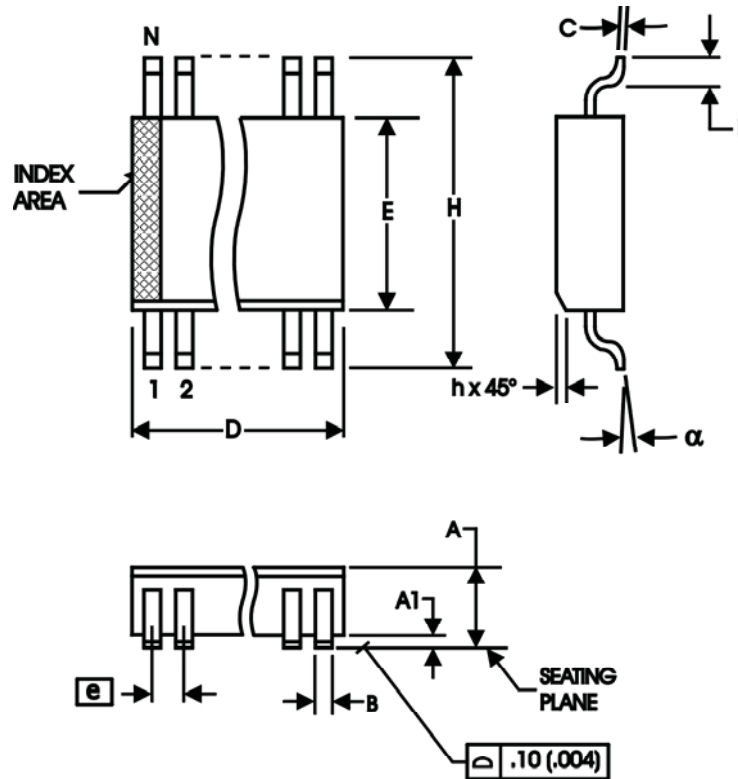


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
$\alpha$	0°	8°

Reference Document: JEDEC Publication 95, MS-012

**TABLE 8. ORDERING INFORMATION**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Shipping Package</b>	<b>Temperature</b>
ICS85222AM-02LF	5222A02L	8 Lead "Lead-Free" SOIC	tube	0°C to 70°C
ICS85222AM-02LFT	5222A02L	8 Lead "Lead-Free" SOIC	tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A		5 6-7	Added <i>Schematic Example</i> . Power Considerations - corrected power dissipation in calculations.	7/24/06
B	T1 T2 T3B	1 2 2 3	Updated Block Diagram with Pulldown for CLK. Pin Description - changed pin 7 as Pulldown instead of Pullup. Changed note to reflect Pulldown. Pin Characteristics - changed Pullup Resistor to Pulldown. LVCMOS DC Characteristics Table - changed $I_{IH}$ from 5 $\mu$ A max. to 150 $\mu$ A max. and changed $I_{IL}$ from -150 $\mu$ A min. to -5 $\mu$ A min.	9/12/07
B	T8	10 1	Ordering Information - removed leaded devices. Features Section - removed reference to leaded devices. Updated data sheet format.	6/15/15

**Corporate Headquarters**

6024 Silver Creek Valley Road  
San Jose, California 95138

**Sales**

800-345-7015 or +408-284-8200  
Fax: 408-284-2775  
www.IDT.com

**Technical Support**

**email:** [clocks@idt.com](mailto:clocks@idt.com)

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners.

Copyright 2015. All rights reserved.