

## Purpose

The RT7272B is a high-efficiency current mode synchronous step-down regulator that can deliver up to 3A output current from a wide input voltage range of 4.5V to 36V. This document explains the function and use of the RT7272B evaluation board (EVB) and provides information to enable operation and modification of the evaluation board and circuit to suit individual requirements.

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## Introduction

### General Product Information

#### General Description

The RT7272B is a high efficiency, current mode synchronous step-down DC/DC converter that can deliver up to 3A output current over a wide input voltage range from 4.5V to 36V. The device integrates a 150mΩ high side and an 80mΩ low side MOSFET to achieve high conversion efficiency up to 95%. The current mode control architecture supports fast transient response and uses a simple compensation circuit.

A cycle-by-cycle current limit function provides protection against a shorted output and an internal soft-start eliminates input surge current during start-up. The RT7272B provides complete protection functions such as input under voltage lockout, output under voltage protection, over current protection and thermal shutdown.

The RT7272B is available in the thermal enhanced SOP-8 (Exposed Pad) package.

#### Features

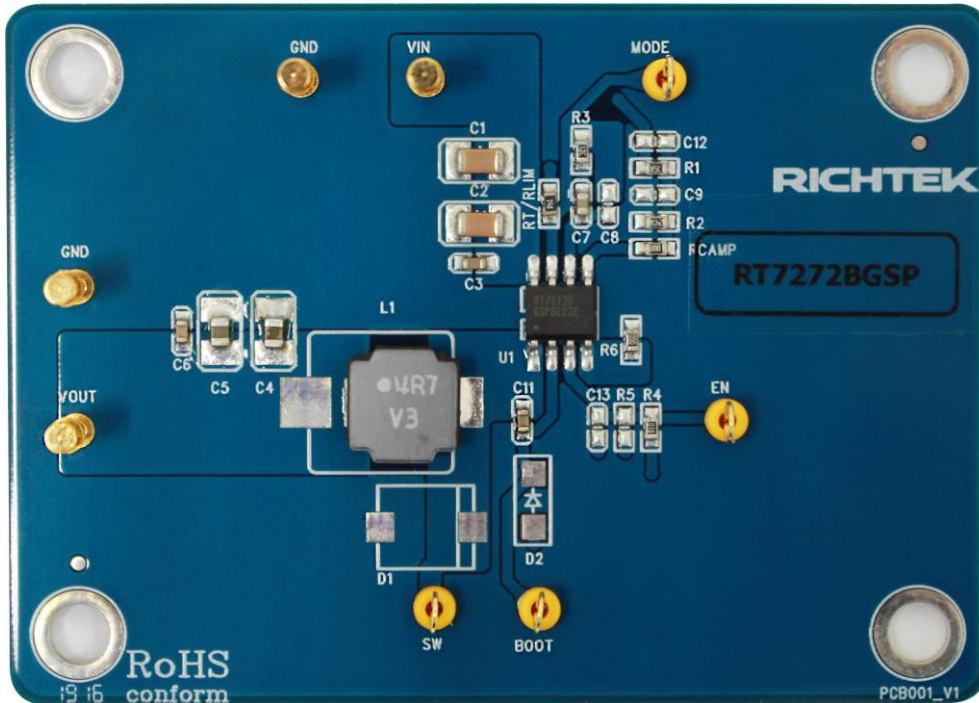
- 4.5V to 36V Input Voltage Range
- 3A Output Current
- Internal N-MOSFETs
- Current Mode Control
- Fixed Frequency Operation : 500kHz
- Adjustable Output Voltage from 0.8V to 30V
- High Efficiency Up to 95%
- Stable with Low ESR Ceramic Output Capacitors
- Cycle-by-Cycle Current Limit
- Adjustable Current Limit

### Key Performance Summary Table

| Key features                   | Evaluation board number: PCB001_V1   |
|--------------------------------|--|
| Default Input Voltage          | 12V  |
| Max Output Current             | 3A (OCP level set to 5.5A typical by $R_{LIM} = 137k\Omega$ )  |
| Default Output Voltage         | 3.3V   |
| Default Marking & Package Type | RT7272BGSP, SOP-8 (Exposed Pad)  |
| Operation Frequency            | Steady 500kHz at PWM   |
| Other Key Features             | 4.5V to 36V Wide Input Voltage Range<br>Adjustable Current Limit 2A to 6A<br>PSM/ PWM Auto Switched.                         |
| Protection                     | Over Current Protection &<br>Output Under-Voltage-Protection (hiccup mode)<br>Input Under-voltage Lock-out, Thermal Shutdown |

## Bench Test Setup Conditions

### Headers Description and Placement



Please carefully inspect the EVB IC and external components, comparing them to the following Bill of Materials, to ensure that all components are installed and undamaged. If any components are missing or damaged during transportation, please contact the distributor or send e-mail to [evb\\_service@richtek.com](mailto:evb_service@richtek.com).

### Test Points

The EVB is provided with the test points and pin names listed in the table below.

| Test point/<br>Pin name | Signal                       | Comment (expected waveforms or voltage levels on test points)   |
|-------------------------|------------------------------|---|
| VIN                     | Input voltage                | Input voltage range= 4.5V to 36V  |
| VOUT                    | Output voltage               | Default output voltage = 3.3V<br>Output voltage range= 0.8V to 30V<br>(see " Output Voltage Setting" section for changing output voltage level) |
| SW                      | Switching node test point    | SW waveform   |
| EN                      | Enable test point            | Enable signal. EN is automatically pulled high (by R4) to enable operation.<br>Connect EN low to disable operation.                             |
| BOOT                    | Boot strap supply test point | Floating supply voltage for the high-side N-MOSFET switch   |
| MODE                    | RLIM test point              | Current limit setting point   |
| GND                     | Ground                       | Ground  |

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## *Power-up & Measurement Procedure*

1. Apply a 12V nominal input power supply ( $4.5V < V_{IN} < 36V$ ) to the VIN and GND terminals.
2. The EN voltage is pulled to logic high by R4 (100kΩ to VIN) to enable operation. Drive EN high (>2.0V) to enable operation or low (<0.4V) to disable operation.
3. Verify the output voltage (approximately 3.3V) between VOUT and GND.
4. Connect an external load up to 3A to the VOUT and GND terminals and verify the output voltage and current.

## *Output Voltage Setting*

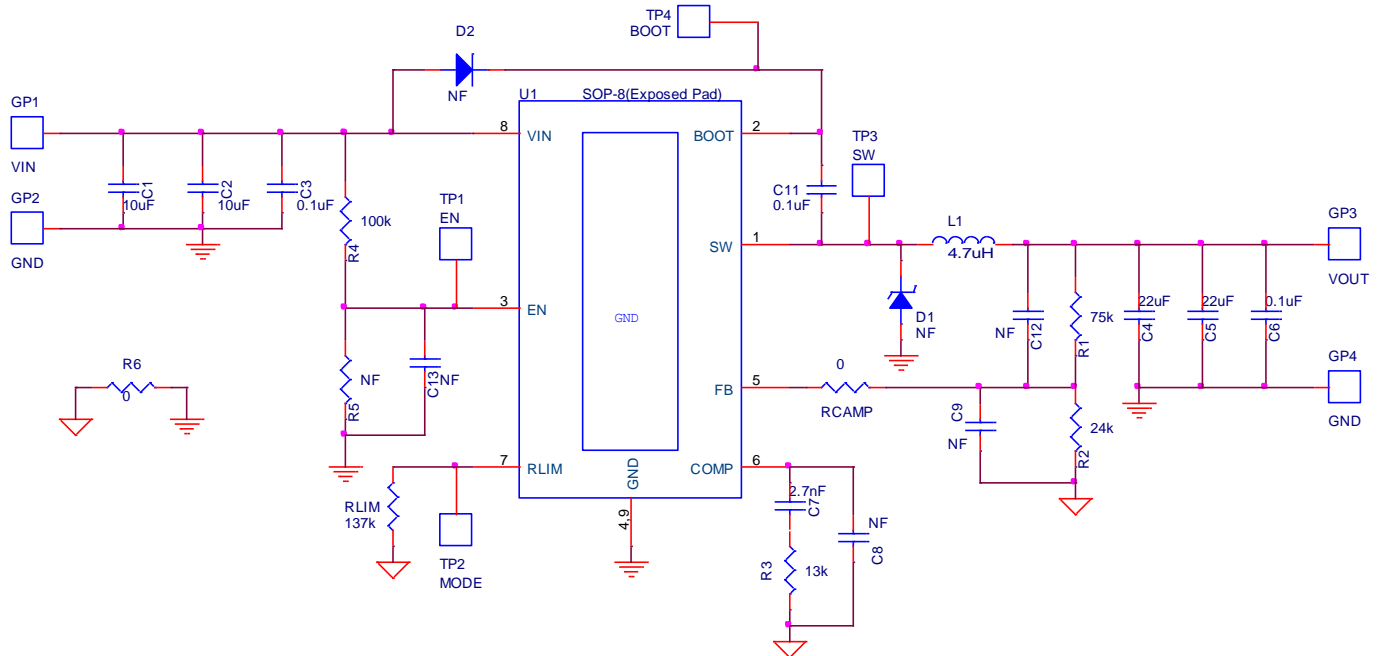
Set the output voltage with the resistive divider (R1, R2) between VOUT and GND with the midpoint connected to FB through RCAMP. The output is set by the following formula:

$$V_{OUT} = 0.8 \times \left(1 + \frac{R1}{R2}\right)$$

The installed  $V_{OUT}$  capacitors (C4, C5) are 22μF, 16V X5R ceramic types. Do not exceed their operating voltage range and consider their voltage coefficient (capacitance vs. bias voltage) and ensure that the capacitance is sufficient to maintain stability and provide sufficient transient response for your application. This can be verified by checking the output transient response as described in the RT7272B IC datasheet.

## Schematic, Bill of Materials and Board Layout

### EVB Schematic Diagram



C1, C2: 10 $\mu$ F/50V/X5R, 1206, TDK C3216X5R1H106K

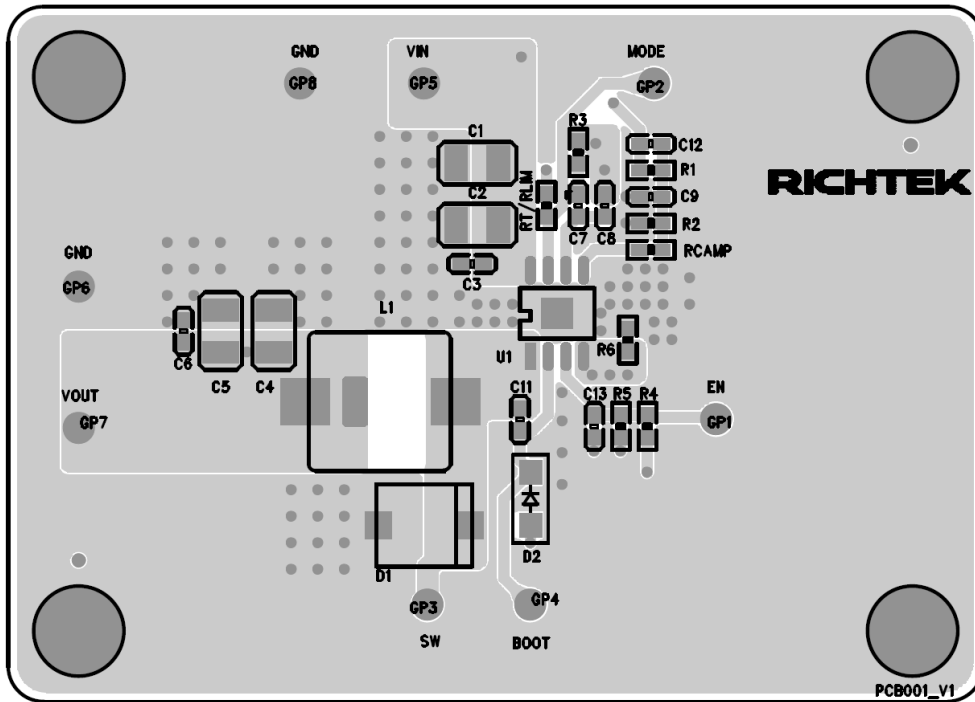
C4, C5: 22 $\mu$ F/16V/X5R, 1210, Murata GRM32ER61C226K

L1: 4.7 $\mu$ H WE74437368047, DCR=15m $\Omega$

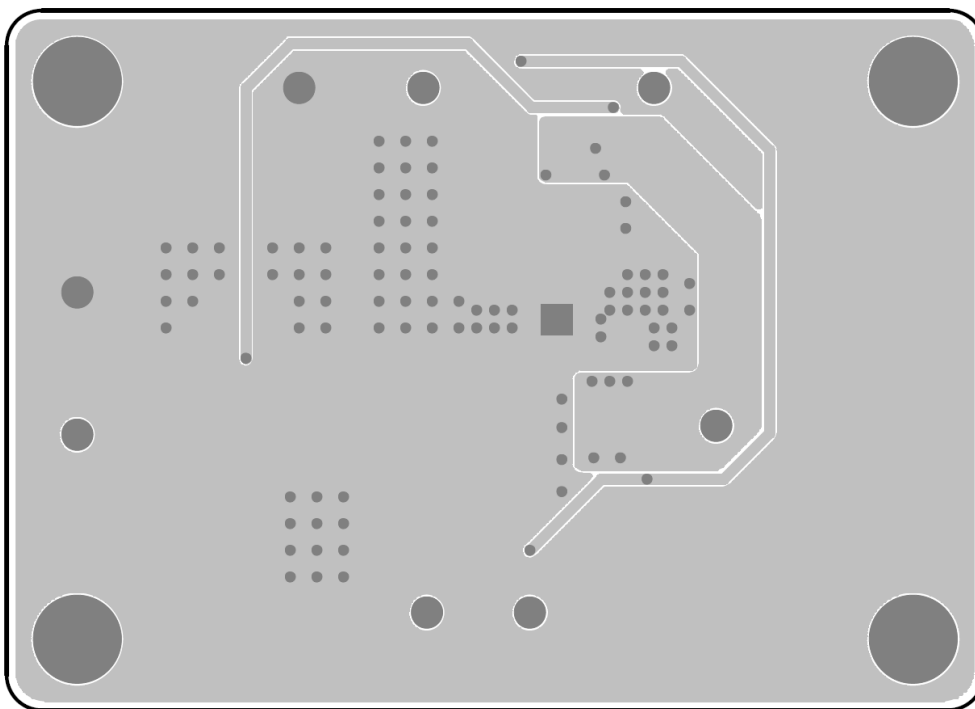
*Bill of Materials*

| Reference        | Qty | Part number         | Description   | Package             | Manufacture |
|------------------|-----|---------------------|---|---------------------|-------------|
| U1               | 1   | RT7272BGSP          | DC/DC Converter   | PSOP-8              | Richtek     |
| C1, C2           | 2   | C3216X5R1H106K160AB | 10 $\mu$ F/ $\pm$ 10%/50V/X5R<br>Ceramic Capacitor          | 1206                | TDK         |
| C4, C5           | 2   | GRM32ER61C226KE20#  | 22 $\mu$ F/ $\pm$ 10%/16V/X5R<br>Ceramic Capacitor          | 1210                | Murata      |
| C7               | 1   | 0603B272K500        | 2.7nF/ $\pm$ 10%/50V/X7R<br>Ceramic Capacitor               | 0603                | WALSIN      |
| C3, C6, C11      | 3   | C1608X7R1H104K080AA | 0.1 $\mu$ F/ $\pm$ 10%/50V/X7R<br>Ceramic Capacitor         | 0603                | TDK         |
| C8, C9, C12, C13 | 0   |                     | Not Installed   | 0603                |             |
| L1               | 1   | NR8040T4R7N         | 4.7 $\mu$ H/4.1A/ $\pm$ 30%,<br>DCR=18m $\Omega$ , Inductor | 8.00mm x 8.00mm     | TAIYO YUDEN |
|                  |     | WE74437368047       | 4.7 $\mu$ H/19A/ $\pm$ 20%,<br>DCR=15m $\Omega$ , Inductor  | 11mm x 10mm x 3.8mm | WE          |
| R1               | 1   |                     | 75k $\Omega$ / $\pm$ 1%, Resistor                           | 0603                |             |
| R2               | 1   |                     | 24k $\Omega$ / $\pm$ 1%, Resistor                           | 0603                |             |
| R3               | 1   |                     | 13k $\Omega$ / $\pm$ 1%, Resistor                           | 0603                |             |
| R4               | 1   |                     | 100k $\Omega$ / $\pm$ 1%, Resistor                          | 0603                |             |
| R5, D1, D2       | 0   |                     | Not Installed   |                     |             |
| R6, RCAMP        | 2   |                     | 0 $\Omega$ , Resistor                                       | 0603                |             |
| RLIM             | 1   |                     | 137k $\Omega$ / $\pm$ 1%, Resistor                          | 0603                |             |
| TP               | 4   |                     | Test Pin  |                     |             |
| GP               | 4   |                     | Golden Pin  |                     |             |

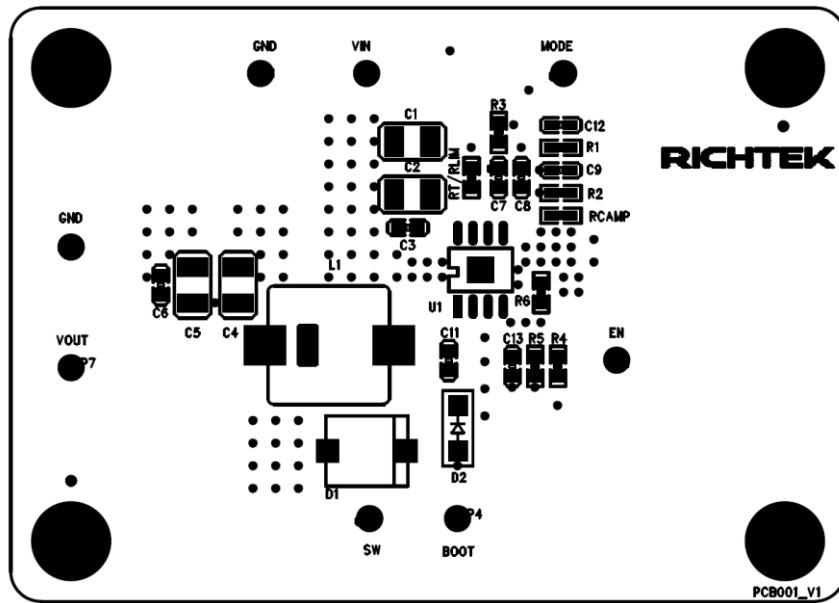
*EVB Layout*



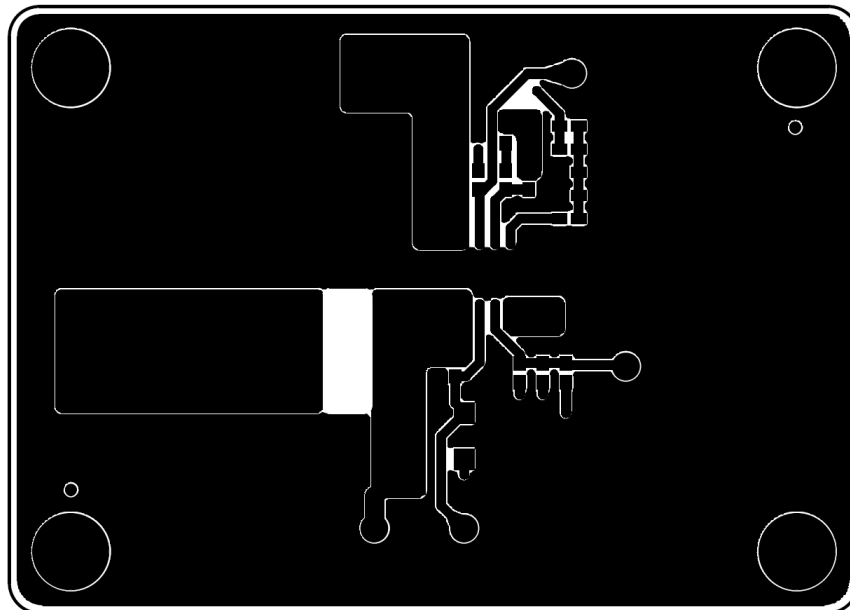
Top View (1<sup>st</sup> layer)



Bottom View (4<sup>th</sup> Layer)

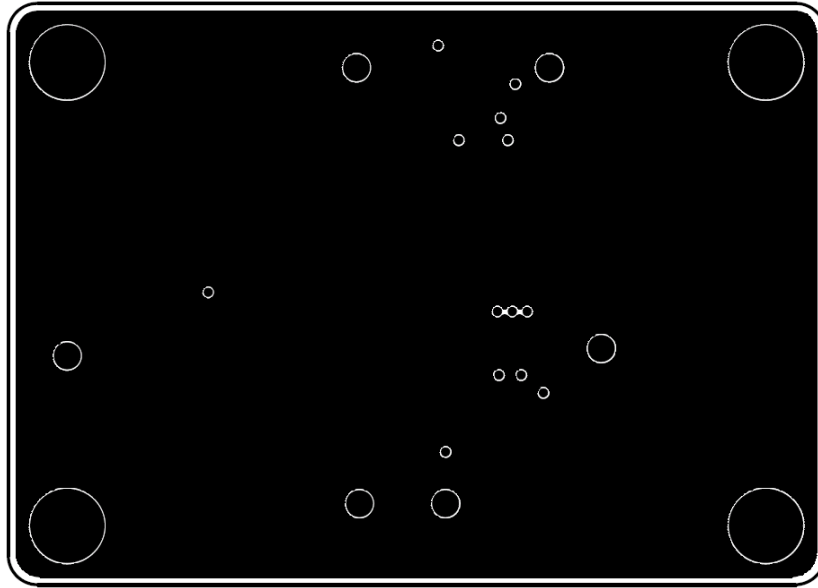


Component Placement Guide—Component Side (1<sup>st</sup> layer)

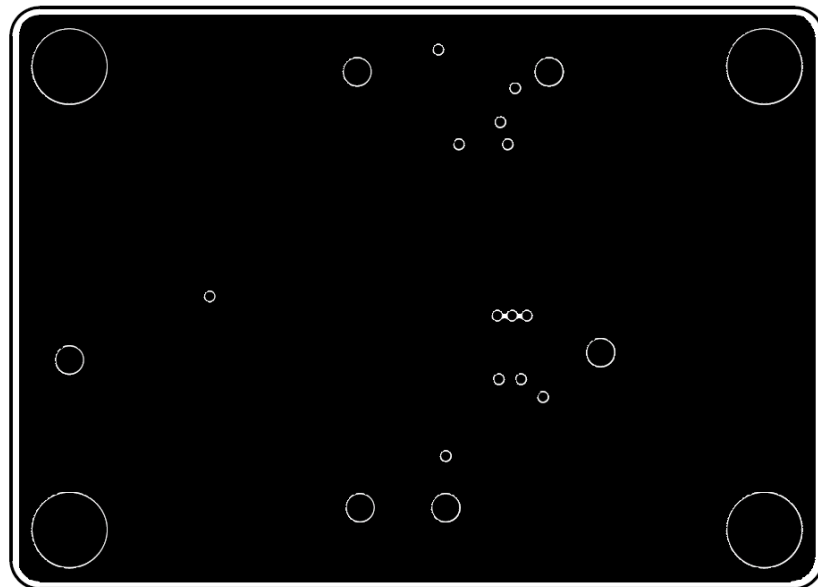


PCB Layout—Component Side (1<sup>st</sup> Layer)

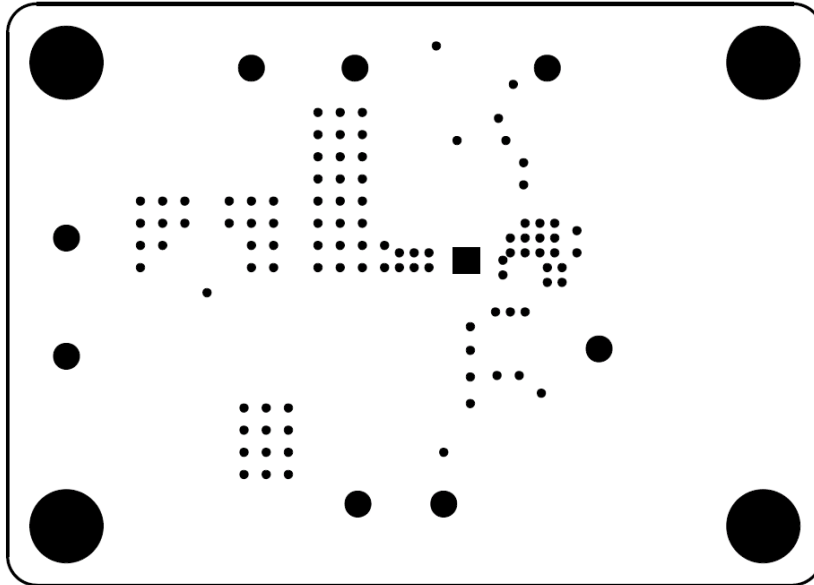




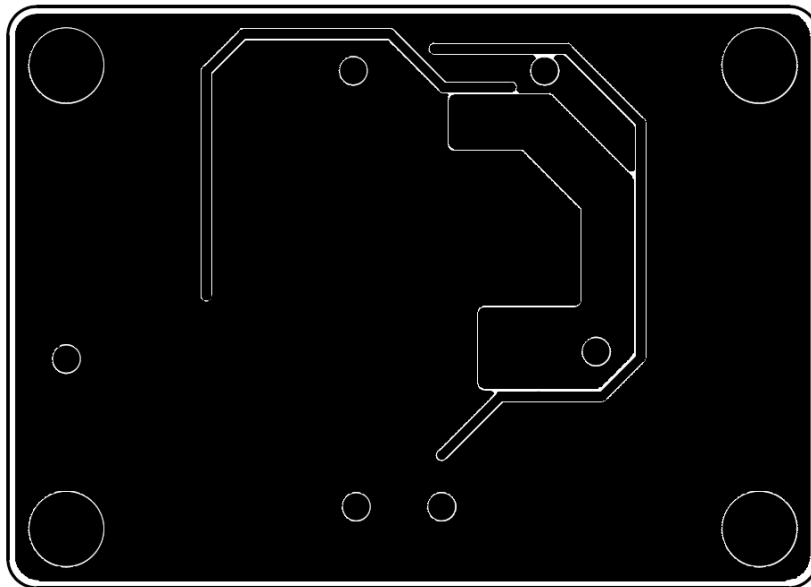
PCB Layout—Inner Side (2<sup>nd</sup> Layer)



PCB Layout—Inner Side (3<sup>rd</sup> Layer)



Component Placement Guide—Bottom Side (4<sup>th</sup> Layer)



PCB Layout—Bottom Side (4<sup>th</sup> layer)

## ***More Information***

For more information, please find the related datasheet or application notes from Richtek website <http://www.richtek.com>.

## ***Important Notice for Richtek Evaluation Board***

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